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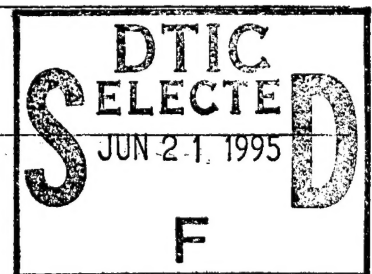
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**Final report to the Air Force Office of Scientific Research  
on a grant F49620-92-J-0096**

**“Novel Hybrid Superconductor/Semiconductor  
Heterostructure Devices”**

**October 1, 1991-September 30, 1994**

**Principal Investigators: A. Kastalsky (AT&T Bell Labs and Stony Brook) and  
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Dept. of Physics, SUNY at Stony Brook, NY 11794-3800**

**Introduction:**

The initial proposal argued a case for a research on a combination of superconducting electrodes (films) with sophisticated III-V epitaxial semiconductor structures exhibiting quantum 2-D electron effects. The materials envisioned at that time included In(Ga)As/AlSb epitaxial multilayered structures and Nb films. The dual purpose was to study physics at Superconductor - Semiconductor (Su-Sm) interfaces and to try and create devices of the superconducting FET type with low power dissipation and high transconductance (rate of change of the channel current with the applied gate voltage,  $dI_{CH}/dV_G$ ).

In the previous work on Su-Sm structures (performed principally in Japan and in the US) superconductivity was induced into a short, heavily doped semiconductor channel, and supercurrent through such a channel was (weakly) modulated via a field effect [1]. The device was called SuFET or JosFET; compared to a normal semiconducting FET it lacked in transconductance and gain. In the proposal we argued that devices with high carrier density in the channel can never produce high transconductance and gain, while a device in which the channel is initially undoped, and the gate voltage controls the lateral tunneling probability through the short channel can indeed exhibit desired characteristics.

Another idea based on resonant tunneling in Su-Sm structures was also put forward in the initial proposal and later developed in more detail as a double barrier resonant tunneling structure.

Accordingly, the work which was performed can be classified, without sharp borders, as work relating to physics aspects and to device aspects. In both cases certain material problems and sample-processing problems were encountered and had to be resolved first.

In 1993 part of the effort was re-directed to a project in which high- $T_c$  films containing e-beam Josephson junctions were to be modulated by an electric field via a gate. It seemed reasonable to expect that ‘weak superconductivity’ manifested by Josephson current will

be much more sensitive to the gate modulation than "strong superconductivity" in a regular film. Certain experiments of this type were already reported by Mannhart and others [2]. We hoped to apply our well-developed e-beam junction technique [9] in order to create well-characterized, high quality Josephson weak-links on top of modulating gates.

Although we were unable to observe pair-current modulation, as described in more detail below, this work resulted in the *first successful demonstration of Josephson junctions on Silicon substrates*, which in itself may be very useful and will have a technological future.

### A). Low- $T_c$ work

#### **Experimental techniques:**

Samples were prepared in a complex way: In(Ga)As/InAs and other III-V structures were mainly supplied by IBM and AT&T collaborations with III-V crystal growers (L. L. Chang at IBM and A. Y. Cho at Bell). Metal films (Au at first, Nb later) were deposited by evaporation and sputtering at Bell, Bellcore, and Stony Brook.

The physics was studied mainly via measurements and analysis of the I-V curves across the interface or interfaces of interest, at different temperatures, with or without a gate voltage applied.

The first challenge was to prepare an FET-type structure with metal (superconducting) source and drain having an ohmic contact to a short channel. This was achieved via angled deposition of a second metal contact using the first one as a shadow mask (Fig. 1a). SEM study revealed 20-40 nm gaps between the two metal films. The yield of non-shortcd samples was up to 80% for 40 nm channel length, and about 50% for 20 nm channel length. A typical SEM photograph depicting a narrow gap between metal banks is shown in Fig. 1b. Most of this initial work was done with non-superconducting (Au) metals in order to develop the sample preparation technique and to study the resulting device in the normal state.

Preparation of shallow ohmic (free of Schottky barriers) contacts at the Su-Sm interface has been recognized for some time as a notorious problem in this field [3]. Indeed, a Schottky barrier between the source (drain) and the channel will prevent pairs from entering (leaving) the channel. We will comment on that problem below; it was largely avoided by using III-V materials with natural conducting surface layer.

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### Ballistic FET:

It turned out that resulting short-channel FETs, even with non-superconducting source and drain, were interesting in their own right [4]. The device structure and the corresponding energy diagram are shown in Fig. 1c. It contains top 10 nm layer of highly doped InGaAs (not shown) provided to improve the ohmic contact. This thin overlayer is followed by a 40 nm of undoped InGaAs which represents the 2-D channel, and a 200 nm InAlAs barrier layer. The  $n^+$  InP substrate serves as a gate for modulating carrier density at the InGaAs/InAlAs interface (see energy diagram in Fig. 1c). This is the so-called "back gate" which is required in order to free the top surface for metal electrode evaporation and short-channel manufacturing.

Measurements of both drain and gate current provided clear evidence of ballistic electron propagation along the channel, i.e. electron scattering time was found to be larger than the time to fly across the channel with Fermi velocity. This produces charge accumulation near the drain, and correspondingly it was found that the current to the gate originates from the drain region of the device. Other unique features include saturation of the drain current at small drain voltages  $V_D < 0.2$  V (Fig. 2a) and a superlinear increase in  $I_D$  with the gate bias  $V_G$  (Fig. 2b). These two phenomena were explained [4] by a poor electron energy-momentum exchange between the 2-D channel and the bulk 3-D electrode.

### Properties of single Su-Sm contacts:

A new phenomenon of a proximity effect-induced pair current has been observed in the Nb/  $n^+$  InGaAs contacts [5, 6]. Additionally, a wealth of new phenomena manifested themselves on Nb/InGaAs and Nb/InAs junctions.

The structure consisted of 200 nm Nb film deposited over a heavily doped 300 nm InGaAs grown on  $n^+$  InP substrate.

a). We observed current deficit in the I-V characteristic which was previously observed only in symmetrical SINIS structures. The explanation previously proposed relied on that symmetry through evoking multiple elastic scattering events in the normal N region. The new results strongly suggested that the current deficit is the intrinsic property of a single Su-Sm interface.

b). Resistance of the Su-Sm interface was found to abruptly increase by about 5% as the temperature is lowered through the  $T_c$  of Nb. As  $T_c$  was suppressed by the magnetic field, the jump moved down in temperature but did not change in magnitude.

c). Another abrupt resistance increase was found at a lower temperatures of 3.5-4K, and this time proved to be very sensitive to applied magnetic field, disappearing at about  $B=0.1$  T. This second effect was ascribed to proximity-induced superconductivity inside the semiconductor.

In addition, the shape of conductance curves at zero bias (zero bias anomaly) further suggests the proximity induced pair currents across the interface, especially in Nb/  $n^+$  InAs where this effect is strongest.

#### **New double-barrier resonant tunneling (DBRT) structure:**

Fig. 3 shows the structure which was conceived and prepared experimentally in order to study resonant Cooper pair tunneling. Thin (1.5 nm) lattice matched GaSb or AlSb barriers separated by a distance of about 6 nm (quantum well, QW) were grown within the low-doped p-type InAs bulk material. The InAs surface provides an inversion layer with high-mobility 2-D electron gas: a well-known consequence of the Fermi level pinning at the surface above the conduction band edge. As a result, the current between Nb contacts flows entirely within a 2-D surface channel shown in dashed lines on the figure. The current then must traverse two resonant tunneling barriers. The energy band diagram at the device surface (Fig. 2b) is similar to a conventional DBRT diagram; the principal difference is in that the emitter and the collector are 2-D channels, while the quantum well (QW) is a 1-D wire.

Biasing the p-type InAs substrate relative to one of the Nb contacts (i.e. biasing of the bulk-to-surface p-n junction) will vary the energy positions of the quantum levels in the channel. This feature is extremely useful in the study of transistor action, three-terminal switching, and resonance tuning. If the ground state energy  $E_0$  in the QW is tuned to coincidence with the Fermi level for zero bias with respect to Nb contacts (Fig. 3b), then, due to resonant tunneling, there will be a supercurrent through the device with the amplitude controlled by the p-n junction bias. The predicted I-V characteristic, shown in Fig. 3c, is expected to contain a superconducting peak at  $V=0$ , followed by a single particle tunneling feature. At larger voltages,  $V=V_R$ , another resonant peak corresponding to injection into the first excited level  $E_1$  will appear. At that time a strong enhancement of the supercurrent will occur giving rise to a large AC Josephson current component with the frequency  $\omega = 2(E_1 - E_0) / \hbar$ . Further, since the device conductance is governed by the 2-D surface channel, Josephson junction capacitance will be much lower than in the case of a conventional sandwich-type device. These new features can be of value to superconducting electronics.

The most essential element of the device processing is the self-aligned deposition of the second Nb contact (Fig. 3a). An efficient high-yield procedure for manufacturing these devices was worked out. First, a 200 nm thick Nb was deposited on the entire wafer surface which was sputter cleaned by Ar for 30 seconds in order to remove native oxide. It was followed by a deposition of 40 nm thick SiO insulator. Then photolithography was used to define 20x20 micron mesa areas, and the rest of the exposed surface was treated in a  $CF_4$  -  $O_2$  plasma etch which removes Nb and SiO from the exposed area of the pattern. After the 100 nm deep etch of the mesa area, 10x10 micron holes are opened in SiO to provide contact to the top Nb layer (N1 on Fig. 3a). Finally, the second 60 nm Nb layer,

Nb<sub>2</sub> is deposited. The yield of good samples was 70% in this processing procedure. One of the most essential features of the resultant structure is the absence of the Schottky barrier at the InAs surface which allows for low-resistance Nb/InAs ohmic contacts to the surface channel.

The first experimental observation of the surface supercurrent was obtained on this structure. The I-V curve for such a device taken at 1.2 K is shown in Fig. 4. A finite current at  $V=0$  manifesting supercurrent through the channel is clearly observed (see the blow-up of the I-V on the right side of the Figure). At  $V=0.15$  V there is a sharp current drop associated with the resonant tunneling process. Thus both superconductivity and resonant tunneling are present in this device. The AC Josephson current in the region of the current drop was not detected so far.

A 10 % decrease of the supercurrent was observed upon the application of the 0.3 V to the substrate, indicating a resonant nature of the supercurrent. This is the preliminary result; it could not be fully confirmed via application of larger positive and negative voltages due to a p-n junction leakage.

The small negative differential resistance amplitude observed in our measurements indicates the presence of carriers in the QW, due to an existence of an inversion layer which penetrates the QW. The same reason prevents effective modulation of the device characteristics by the gate bias: the Fermi level is pinned in the QW at the surface. In order to eliminate this problem one would need to prepare the QW from  $\text{In}_{0.77}\text{Ga}_{0.23}\text{As}$ . Indeed, the linear interpolation between the  $\text{In}_{0.47}\text{Ga}_{0.53}\text{As}$  composition having a Schottky barrier of 0.25 eV at the surface, and InAs having an accumulation layer at the surface, yields a flat band (neither depletion nor accumulation at the surface) for  $\text{In}_{0.77}\text{Ga}_{0.23}\text{As}$ . In this case one should observe much more pronounced resonant tunneling component and the gate modulation.

### **B). High- $T_C$ work:**

As was said in the Introduction, in 1993 part of the effort was re-directed toward a study of field effect on SNS-type electron beam-prepared Josephson junctions in YBaCuO (YBCO) thin films, first on  $\text{SrTiO}_3$  (STO) substrates, and then on Si/YST substrates.

#### **Attempts to observe field effect on a Josephson current in SNS junctions on STO:**

The first series of experiments aimed at creating SNS-type Josephson junctions which could be modulated by the electric field. They were conducted on films grown on doped STO.

The doping was performed via laser annealing of Nb films pre-deposited on an STO substrate, as shown in Fig. 5a. Previous work [7] have shown that such a procedure can produce thin (200 nm) surface layer embedded in STO, said layer having metallic conduction, and in fact even exhibiting superconductivity below typical doped-STO



transition temperatures of less than 1K. The geometry of the doped region is determined by the lithographically defined geometry of the deposited Nb film. After the pulsed laser anneal (which was performed using CO<sub>2</sub> laser) extra Nb was stripped in a plasma etching system in CF<sub>4</sub> atmosphere or by liquid etching, leaving a doped layer of STO (Fig. 5b).

The (quasi-epitaxial) YBCO film was grown on top of this structure at Bell Labs using the BaF<sub>2</sub> (Mankiewich) process. Films were prepared in Julia M. Phillips' group, by Shang Hou [8]. Subsequently, the film was patterned in the usual way into the 3-4  $\mu$ m wide bridge geometry and electron beam writing was performed across the film using the technique described in Ref. 9. However, the dose (electron fluence) given the damaged region was such as to suppress all superconductivity and metallic conductivity in it, leaving the only possible supercurrent path through the doped substrate. The gate in a form of metallization layer was placed on the back of STO substrate, relying on the well-known high static dielectric constant of STO to produce considerable charge modulation in the doped N-region (Fig. 5c).

This line of experiments proved rather difficult and was finally abandoned. One problem which was quickly encountered was in the need to post anneal YBCO films in oxygen during the preparation using the BaF<sub>2</sub> process. During this anneal at temperatures exceeding 700-800 C, the Nb doped layer which was pre-arranged on the STO substrate tended to diffuse around; in fact it went right through the 1 mm thick STO substrate and shorted out the gate. Thus any gate-induced modulation became impossible. At the same time the resulting SNS structure did not show any (Josephson or otherwise) supercurrent, probably due to lowered doping in the surface layer and /or non-ohmic contacts between YBCO and that layer.

#### **Gated structures on doped Si substrates:**

Another line of investigation concentrated on Josephson structures prepared on Si substrates: the Si/YSZ/YBCO structures. Here "Si" stands for a standard single-crystalline Si wafer, "YSZ" for a 50 nm thick epitaxial buffer layer of Ytria-stabilized Zirconia, and "YBCO" for a 88-90K laser-ablated epitaxial film 50 nm thick grown on top of YSZ.

These unique high-quality samples were supplied by Peter Rosenthal and his colleagues at Advanced Fuel Research (AFR) Company. In order to be able to investigate field effect on the Josephson current in such structures, we asked the AFR group to grow on heavily doped Si substrate (supplied from Stony Brook). Thus the substrate itself became the gate, with Aluminum metallization on the back serving as a contact to Si, and YSZ serving as the gate insulator.

Unfortunately, the YSZ proved to be leaky (probably due to pinholes). After a number of tries we were able to apply a maximum of 0.4 V to the gate with gate-to-YBCO leakage current being below 50  $\mu$ A. This gate voltage is too small to produce significant charge modulation in the Josephson junction, and we were unable to observe Josephson current modulation in these experiments.

At the same time, transport measurements performed on similar YBCO films blanket-irradiated with electrons showed that, in contrast to our earlier expectations, they have essentially unchanged carrier concentrations, the same as in the original undamaged films. In this case the carrier concentration in the weak-link region is of the order of  $5 \times 10^{21} \text{ cm}^{-3}$  which is too large for significant field modulation even at much higher fields [7].

### Josephson junctions and SQUIDs on Si substrates:

Although field effect did not work as we expected, something good came out of this effort: in the process we, for the first time, prepared good Josephson junctions on buffered Si substrates. Placing HTSC JJs, SQUIDs and circuits on Silicon wafers has immediate and obvious technological appeal. Although this was not a part of our original plan, we report briefly on this work which became possible due to the support we received from the AFSC on this grant. A first publication based on this work (APL) is presently being prepared by our group and Peter Rosenthal. The work continues; we expect it to continue in the future in a form of a study of SQUIDs and small RSFQ circuits on Si.

Here we present the more recent results obtained on a SQUID circuit on Si: these data largely encompass the single junction behavior which was also observed on other samples.

Fig. 6 shows the photograph of a SQUID structure on Si substrate. The loop area is 128 square microns; the two narrow bridges have width of 4 microns each. The processing of this structure involves essentially the same steps as that of a similar structure on other substrates [9]. The liquid etch which defines the YBCO film slows down when it comes to YSZ; the dark background depicts the surface of YSZ.

The critical currents in the two SQUID bridges were not identical, probably due to film inhomogeneities.

We observed RSJ-like I-V characteristics and Shapiro steps at 10.2 GHz as shown in Fig. 7, and magnetic modulation as shown in Fig. 8. The modulation period in terms of the applied current allows us to find the inductance of the line,  $L$ . From the measured  $\Delta I = 50 \text{ } \mu\text{A}$  we find  $L = \Phi_0 / \Delta I = 40 \text{ pH}$ . The total inductance of a SQUID is about 100 pH.

It was found that a significant part of this inductance is kinetic rather than geometrical, i.e. inductance associated with the current energy rather than magnetic field energy. By measuring the period of SQUID oscillations as a function of temperature we obtained the temperature dependence of the inductance, and hence the T-dependence of the London penetration depth,  $\lambda(T)$ . This is a new sensitive method of measuring  $\lambda(T)$  at low temperatures which may be important in view of a recent controversy concerning the pairing state symmetry in HTSC.



## Summary and conclusions:

A). New high-transconductance device concepts were developed, and several new phenomena were observed in Nb/  $n^+$  In(Ga)As junctions.

In particular, current deficit (negative I-V intercept) was observed in a single Su-Sm interface, contrary to the existing model which requires a double Su-Sm-Su structure. An enhancement of the zero bias conductance peak in Nb /n InAS compared to In/InGaAs was observed, supporting pair tunneling as a mechanism for zero bias anomaly.

An angled source-drain deposition technique allowed making transistor structures with less than 40 nm source-to-drain distances. A new (non-superconducting) ballistic short-channel transistor was fabricated and studied.

A new hybrid Su-Sm resonant tunneling device was also conceived and fabricated. Both the supercurrent and the negative resistance (current drop) due to resonant tunneling were observed experimentally. Poor gate isolation hindered further progress, however.

The work performed on this low- $T_C$  part did not produce working high-transconductance hybrid transistors. However it laid ground for future research in this difficult and interesting area of device physics, and resulted in a number of publications.

B). The largely negative results concerning field modulation of Josephson structures in HTSC films were obtained which are nonetheless useful. In particular, in the process of this work it was discovered that carrier density in electron irradiated YBCO does not change significantly, despite large increases in residual resistivity. This hinders attempts at electric field modulation of Josephson structures thus prepared.

Technologically interesting study of Josephson junctions and SQUIDs on Silicon substrates was undertaken as part of this grant. This led to a potentially important spin-off: SQUIDs and active Josephson HTSC circuits on Si.

### **Publications and References:**

1. See for example: T. Kawakami and M. Takayanagi, Appl. Phys. Lett. **46**, 92, (1985); A. W. Kleinsasser, T. N. Jackson, D. McNruff, F. Rammo, G. D. Petit, and J. M. Woddall, Appl. Phys. Lett. **55**, 1909, (1989).
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### **Talks and Seminars:**

APS March Meeting, Seattle, Washington, 1993  
Applied Superconductivity Conference, Boston, 1994

Invited talks and seminars: KFA, Juelich, Germany, 1994  
AT&T Bell Labs, Murray Hill, N.J., 1994  
University of Maryland, 1993

## Figure Captions:

Fig. 1a: Angled metal deposition for manufacturing of short source-drain devices

1b: Device structure

1c: Device energy diagram

Fig. 2a: Drain (solid lines) and gate (dashed lines) currents vs. drain bias.

2b: Drain current vs. gate voltage measured at 4.2 K. The drain current increases  $10^4$  times from 0.4 V to 2 V.

Fig. 3a: Mesa structure of the resonant transistor; dashed line indicates surface 2-D channel.

3b: Device energy band diagram.

3c: The expected I-V characteristic.

Fig. 4: The experimental I-V; on the right: low-voltage part enhanced.

Fig. 5a: Pulsed laser anneal of Nb on the surface of STO

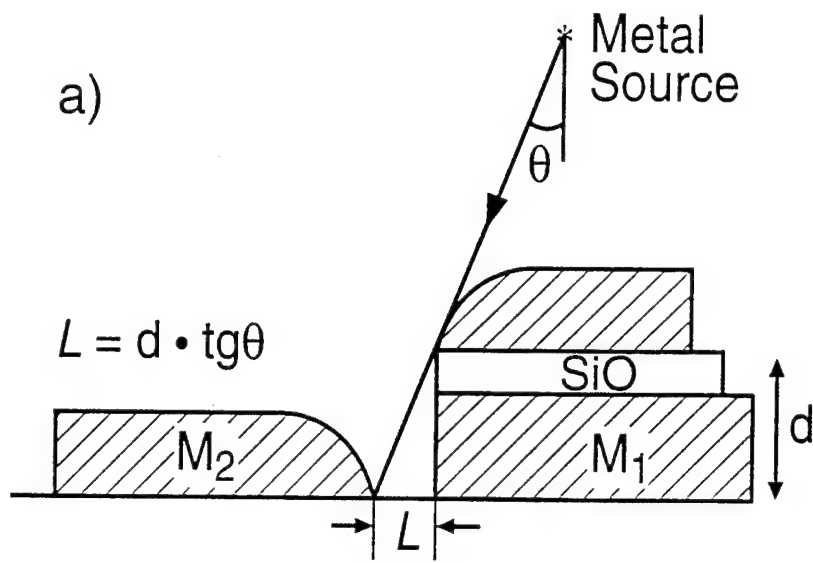
5b: Resulting doped surface layer

5c: YBCO film on top of this structure; narrow region is damaged by electron beam.

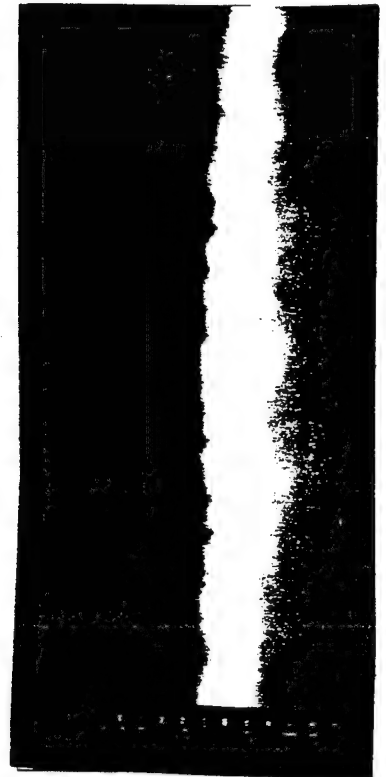
Fig. 6: A photograph of the SQUID structure on Silicon; 4 micron mark is shown.

Fig. 7a: I-Vs of a SQUID at different temperatures and Shapiro steps in the 10.2 Ghz field.

Fig. 8: Magnetic field modulation of the SQUID on Silicon.



b)



c)

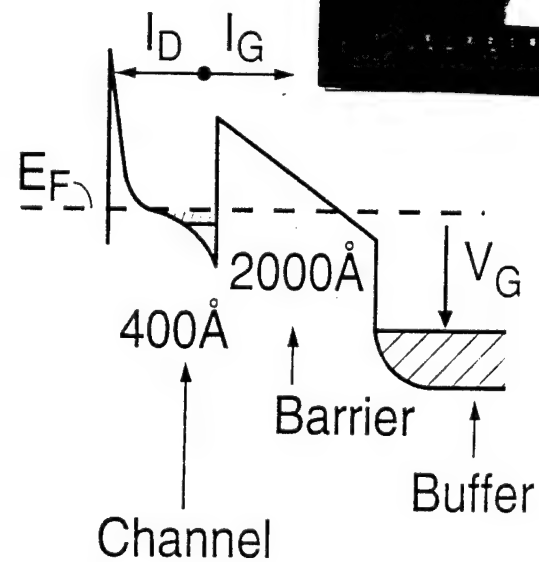
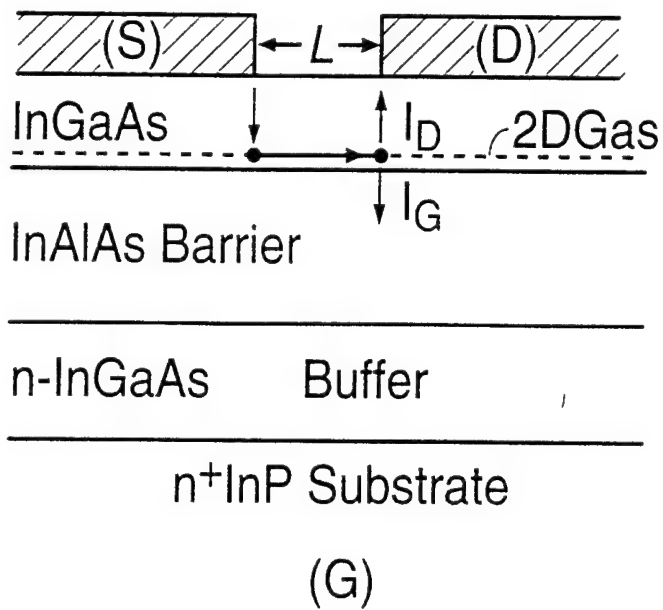
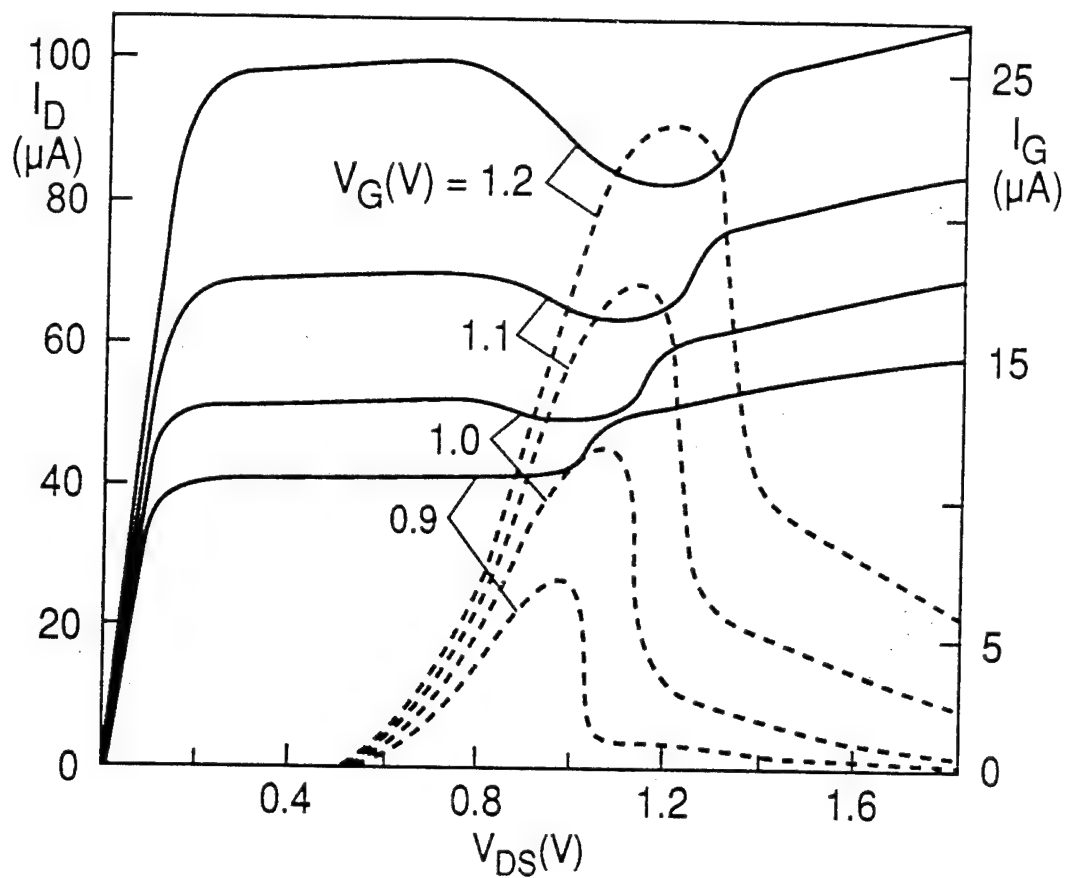


Fig. 1



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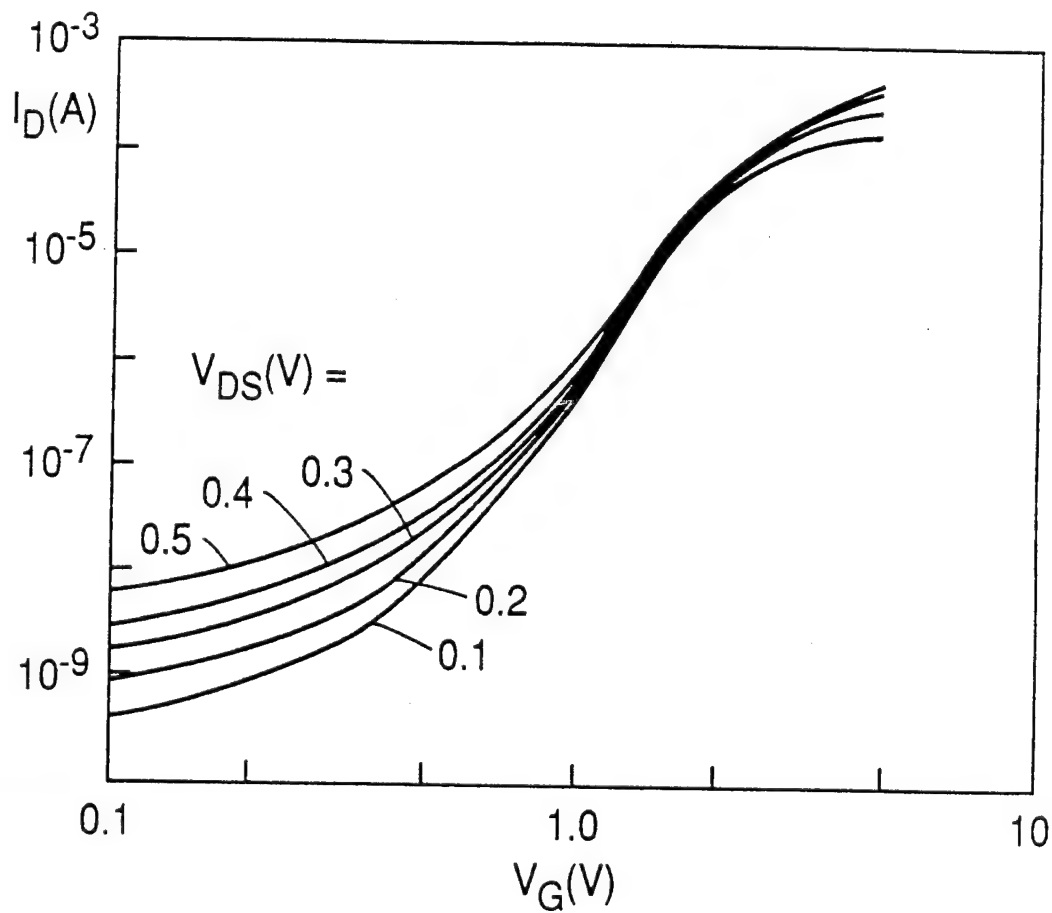
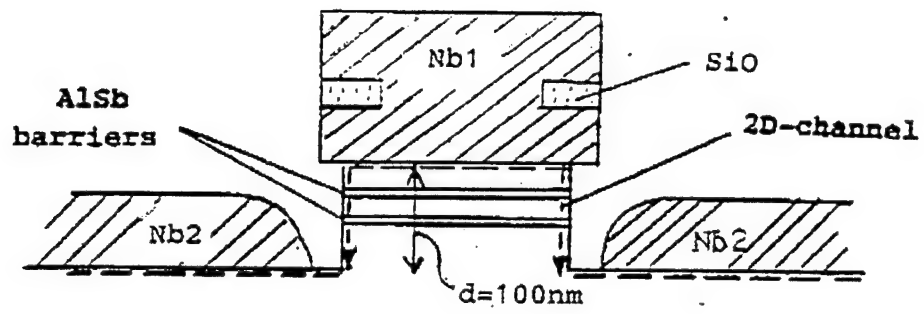
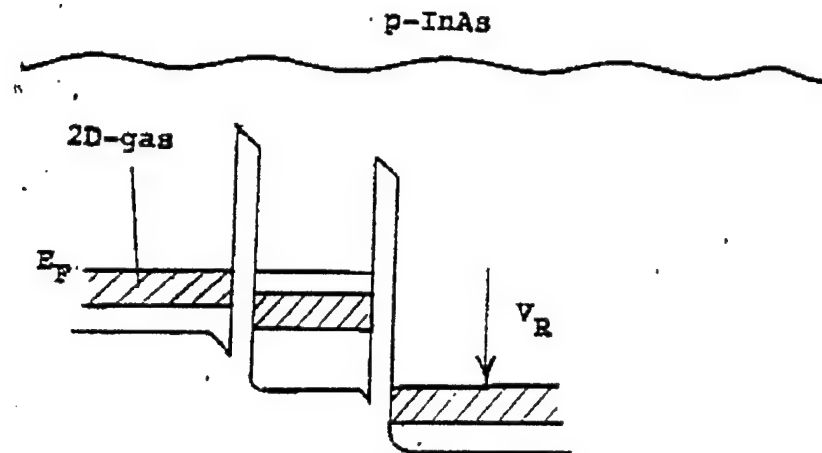


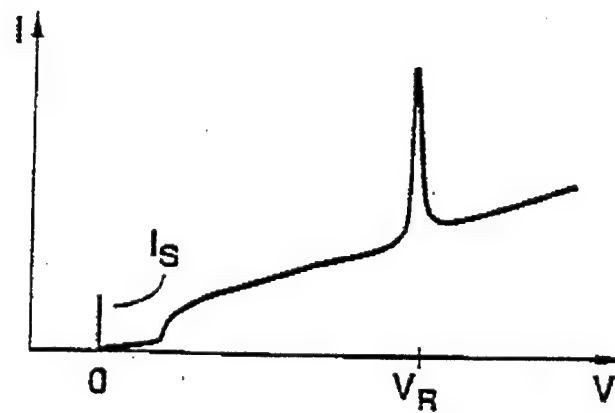
Fig. 2



a)



b)



c)

Fig. 3



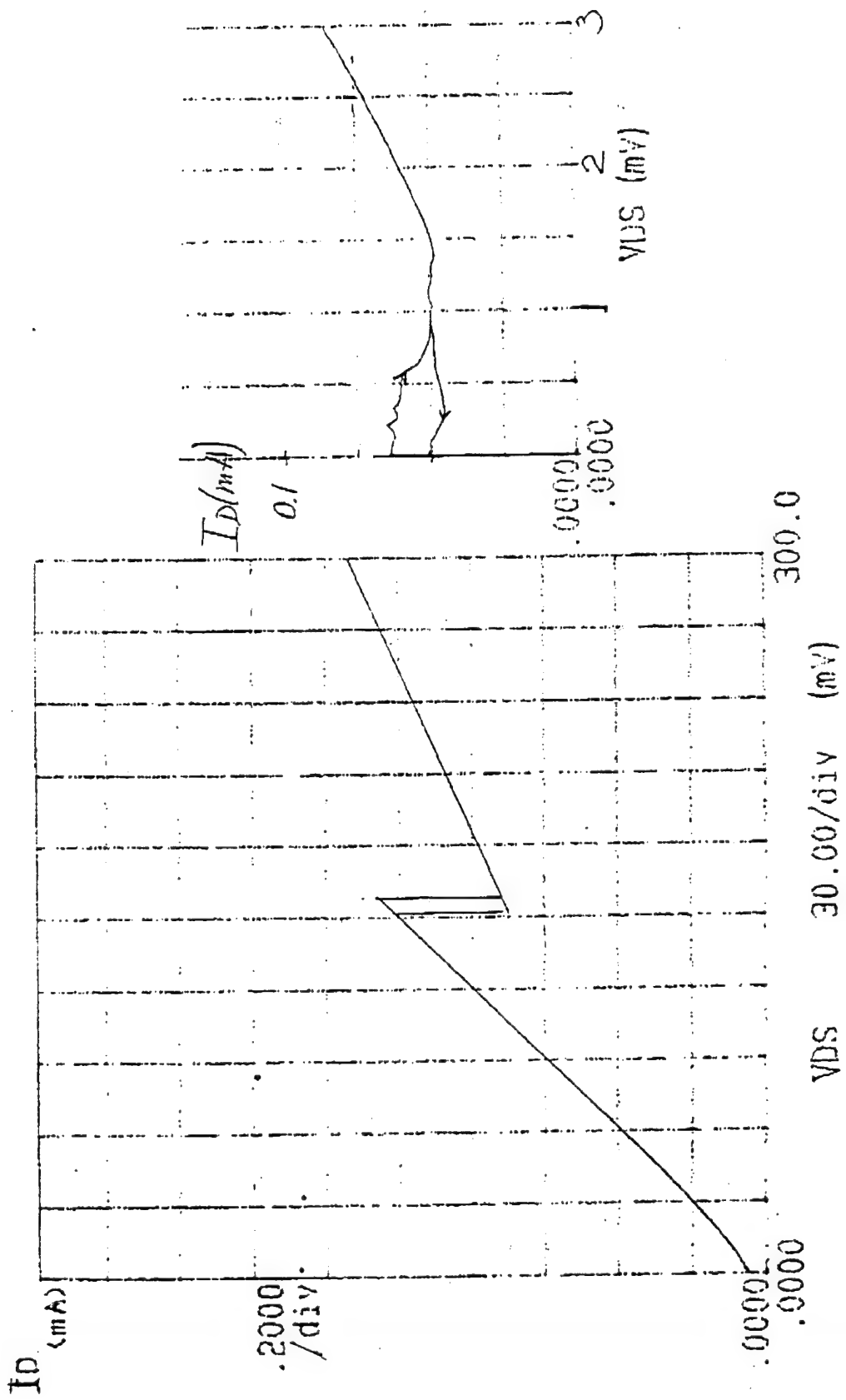


Fig. 4

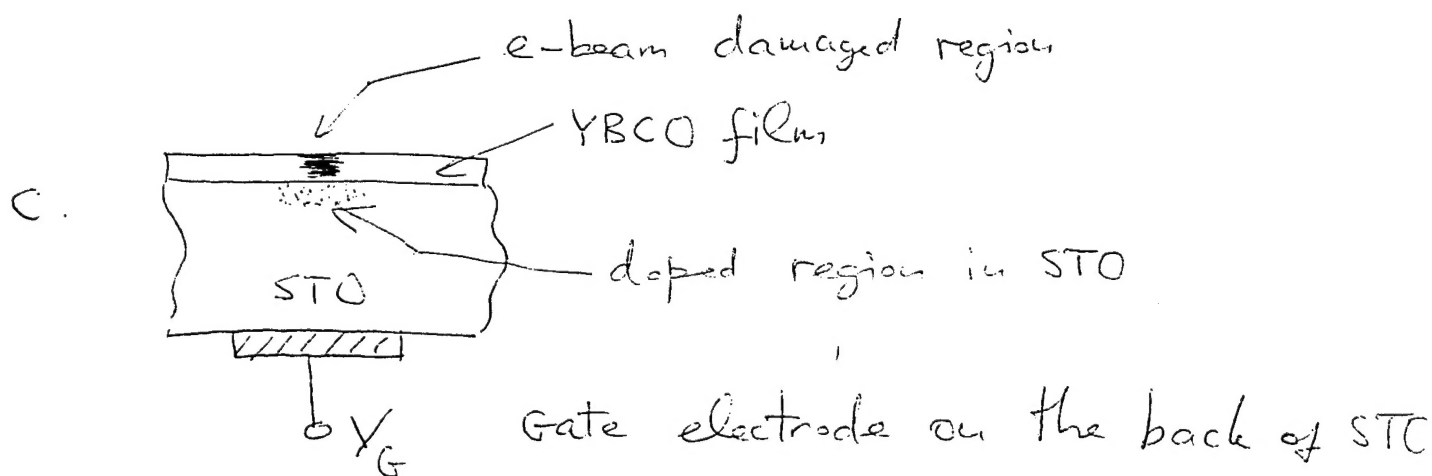
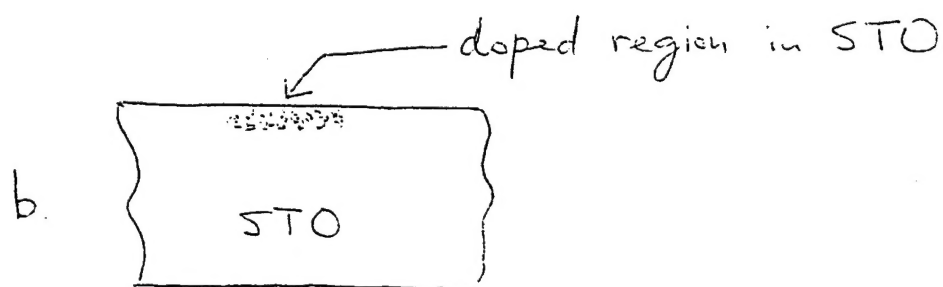
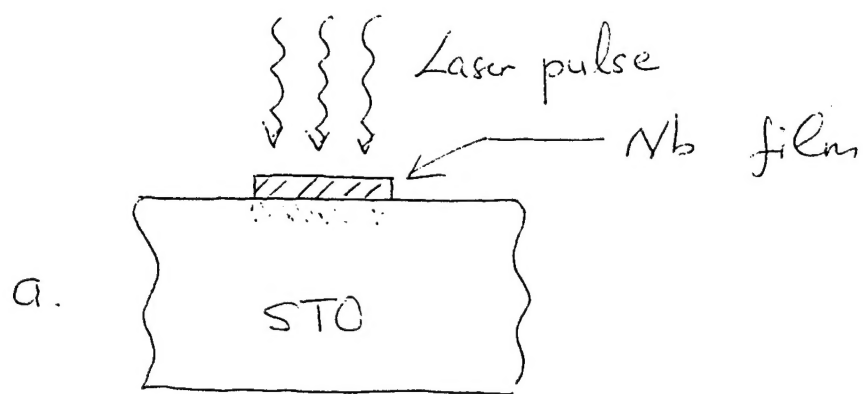
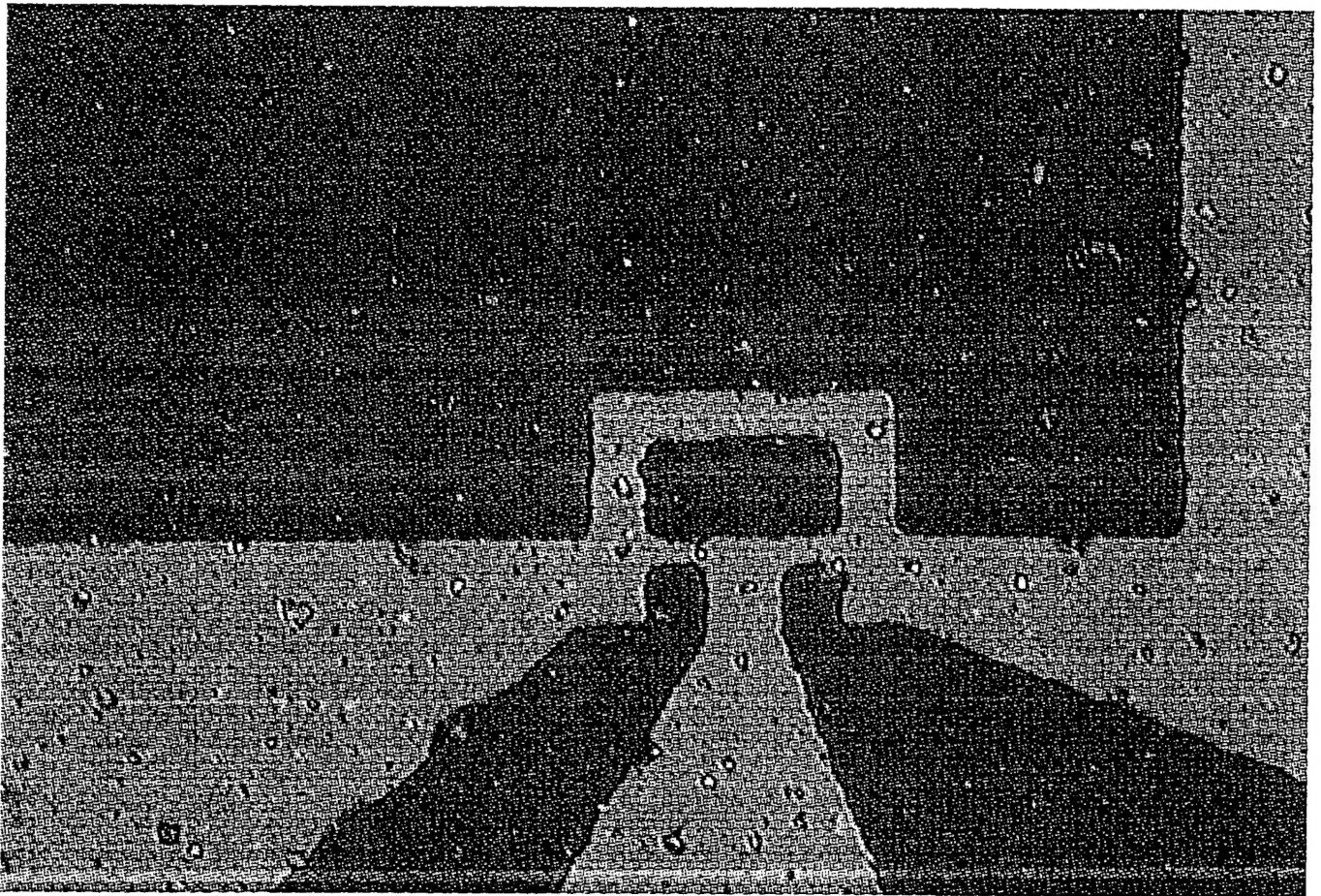


Fig. 5



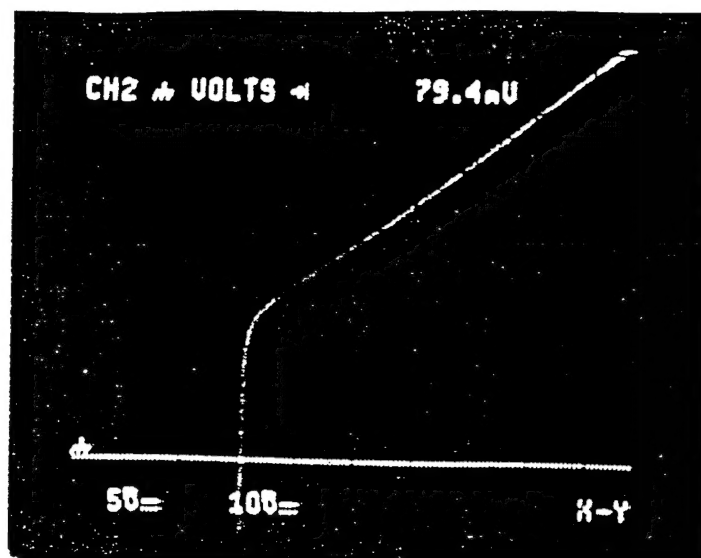
HTS SQUID (YBCO) on silicon substrate

4 mkm

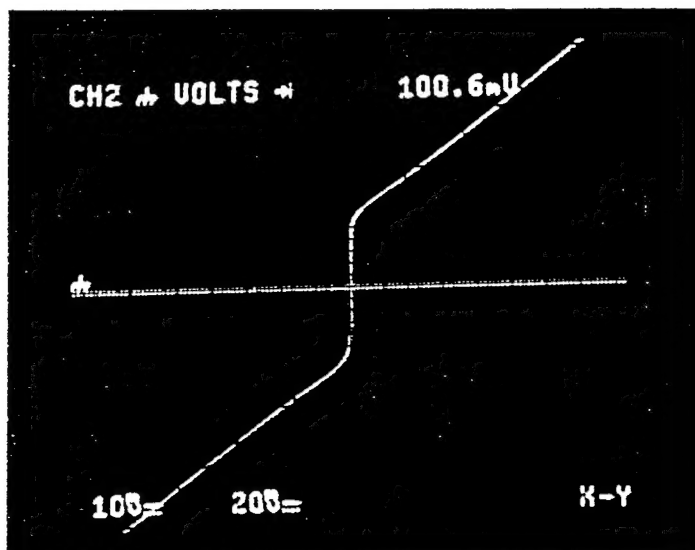
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Fig. 6

T=54 K



T=61 K



T=61 K

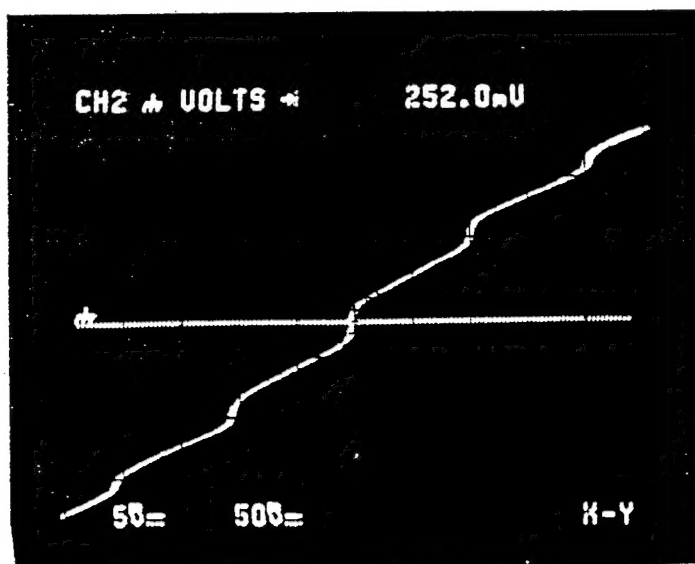


Fig. 7

$T = 32 \text{ K}$



Magnetic modulation of the SQUID R-2. (YBCO SQUID on silicon substrate).

$X = 2 \text{ mV/inch}$

$Y = 100 \text{ mA/inch}$

Fig. 8